EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	205	703/2.ccls. and @pd>"20061201"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 12:19

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S44	1176	verilog and 'define and @ad<"20010901"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 15:49
S45	3	"6813597".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 15:51
S46	3	"6401230".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 15:53
S47	2	"6226780".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 15:54
S48	2	"5841663".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 16:05
S49	2	"6,311,239".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 16:06
S50	2	"5802399".pn.	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 16:06
S51	114	yumoto.in. and @ad>"19980101" and @ad<"20010701"	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/06/21 16:07

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L Bening
E Girczyc
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S Carlson

[BOOK] ... of Verifiable Rtl **Design**: A Functional Coding Style Supporting Verification Processes in **Verilog** - all 6 versions »
L Bening - 2001 - books.google.com
... 2. **Verilog** (Computer hardware description language) 3.Electronic digital ... 6.4.2 Model Checking and **Parameterized** Modules 126 6.4 ... 131 7. 1 **Design** Content 132 7. 1 ...
Cited by 54 - Related Articles - Web Search - Library Search

VHDL & **Verilog** Compared & Contrasted-Plus Modeled Example Written in VHDL, **Verilog** and C. - all 16 versions »
DJ Smith - Proc. 33rd **Design** Automation Conf, 1996 - doi.ieeecomputersociety.org
... reuse, • configuration statements for configuring **design** structure, • generate ... **Verilog**. ... to parameterize models by overloading **parameter** constants, there is ...
Cited by 25 - Related Articles - Web Search - BL Direct

Verischemelog: **Verilog** embedded in Scheme - all 4 versions »
J Jennings, E Beuscher - Proceedings of the 2nd conference on Domain-specific ..., 2000 - portal.acm.org
... **Verilog** has a small macro language, essentially based ... Therefore, although many **designs** are **parameterized**, there are ... Common **design** ele- ments in digital systems ...
Cited by 8 - Related Articles - Web Search - BL Direct

Parameterized IP core **design**
Z Junchao, C Weiliang, W Shaojun - ASIC, 2001. Proceedings. 4th International Conference on, 2001 - ieeexplore.ieee.org
... They are common in the **design** of the control Page 3 ... needs IF providers to support both **Verilog** and VFIDL ... For example, a **parameterized** IF core is designed to ...
Cited by 9 - Related Articles - Web Search

Increasing **design** quality and engineering productivity through **design** reuse - all 2 versions »
E Girczyc, S Carlson - Proceedings of the 30th international conference on **Design** ..., 1993 - portal.acm.org
... Next, **designs** can be **parameterized**. While a ... In an FILD methodology, functionality can also be **parameterized** without increasing **design** cost if ...
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Three decades of HDLs. II. Conlan through **Verilog** - all 6 versions »
D Borrione, R Piloty, D Hill, KJ Lieberherr, P ... - **Design** & Test of Computers, IEEE, 1992 - ieeexplore.ieee.org
... in the mid-1 970s through the development of **Verilog** in the ... evaluate and write as- sertions either after the interface/ **parameter** list of a **design** entity or ...
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Trends in CAD of analog ICs - all 2 versions »
BAA Antao, AD Technol, M Inc, TX Austin - Circuits and Devices Magazine, IEEE, 1996 - ieeexplore.ieee.org

... New develop- ments in AHDLs have seen the emergence of standards for VHDL-A and **Verilog**-A to ... Model **parameter** extraction and **design** methodologies Inadequate ...
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AHD languages-a must for time-critical designs - all 3 versions »
BAA Antao, AD Technol, M Inc, TX Austin - Circuits and Devices Magazine, IEEE, 1996 - ieeexplore.ieee.org
... to be repre- sented, VHDL-A and **Verilog**-A are lan ... is some flexibility to specify the **parameter** values such ... application areas of the analog **design** process where ...
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Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs - all 9 versions »
CE Cummings - SNUG-2001 San Jose, CA Voted Best paper, 2001 - sunburst-**design**.com
... This time window is specified as a **design parameter** precisely to keep a data signal from changing too close to another synchronizing signal that could cause ...
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A System for Evaluating Performance and Cost of SIMD Array Designs - all 14 versions »
MC Herbordt, J Cravy, R Sam, O Kidwai, C Lin - Journal of Parallel and Distributed Computing, 2000 - Elsevier
... program to generate the **designs** in the **Verilog** high-level ... 4. If a **design** to be evaluated has not ... thesized, but is legal for the **parameterized** hardware model ...
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Patents

Patents **1** - **10** on **verilog parameterized design**. (**0.27** seconds)

Apparatus and method for synthesizing integrated circuits using **parameterized** HDL modules ...
US Pat. 5841663 - Filed Sep 14, 1995 - VLSI Technology, Inc.
Kim ("Automatic behavioral **Verilog** model generation using engineering ... ("Guided synthesis and formal verification techniques for **parameterized** hardware ...

Method of generating customized megafunctions
US Pat. 6401230 - Filed Feb 1, 1999 - Altera Corporation
To the **design** compiler, **parameterized** ... a non-**parameterized** functions of a type that may be easily handled (by, for example, VHDL and **Verilog** compilers). ...

Electronic **design** automation apparatus and method utilizing a physical information database
US Pat. 5487018 - Filed Aug 13, 1993 - VLSI Technology, Inc.
This invention more particularly relates to an electronic **design** automation ... for the simple non-**parameterized** datapath cells typically used in the past. ...

FPGA modules **parameterized** by expressions
US Pat. 6216258 - Filed Mar 27, 1998 - Xilinx, Inc.
... hardware **design** languages (hdls) are similar to high level programming ... hdls such as VHDL or **Verilog**, and commonly used hlls such as C++ or Java. ...

Circuit **design** method and apparatus supporting a plurality of hardware **design** languages
US Pat. 6226780 - Filed Aug 31, 1998 - Mentor Graphics Corporation
... From **Parameterized** Schematic **Design** System," IEEE, pp. 130-134, 1997.* Sauge et al., "Integrating of **Verilog**-HDL and VHDL Languages in the SMASH™ ...

Method and apparatus for data path circuit layout **design** and memory medium for causing computer ...
US Pat. 5737237 - Filed Feb 16, 1996 - Matsushita Electric Industrial Co., Ltd.
14 is a flow chart of a data path circuit layout **design** SIS. ... language **Verilog** HDL: The following description will discuss a **parameterized** function ...

Mixed signal synthesis behavioral models and use in circuit **design** optimization
US Pat. 6637018 - Filed Oct 26, 2000 - Cadence Design Systems, Inc.
25 vi- Generate the **parameterized** model. This task has to be executed first. 2-2-1 Synthesis Models **design** knowledge into a Synthesis Plan. ...

Method and apparatus for addressing multiple frame buffers
US Pat. 6411302 - Filed Jan 6, 1999 - Concise Multimedia and Communications Inc.
In VHDL a standard library of **parameterized** modules (LPM) is available. ... components that can also be used to implement the current embodiment is **Verilog**. ...

Mixed signal synthesis
US Pat. 6813597 - Filed Jun 8, 2000 - Cadence Design Systems, Inc.

Generate the **parameterized** model. i. **Parameterized** the circuit netlist.
2.2.1 Synthesis Models 2. Model each performance characteristic in terms of **design ...**

Standard library generator for cell timing model
US Pat. 6496962 - Filed Nov 17, 2000 - LSI Logic Corporation
4 is a more detailed flowchart of the step of expanding the **parameterized ...**
The **Verilog** models may then be distributed as part of an ASIC **design** system. ...

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   Yu, K.M.; Zhu, W.M.;
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